			Previous day											
			JST, KST(UTC+9)			CST, SGT(UTC+8	MSK(UTC+3)	CEST(UTC+2)	EDT(UTC-4)	PDT(UTC-7)				
			Japan, Korea			China, Taiwan, Singapore	Moscow	Central Europe	USA East Coast	USA Pacific Coast				
	Date(JST)	Session #	Start	Finish	Length	Start	Start	Start	Start	Start	Paper #	paper_id	Paper Title	Author Full Names	Organizations
Day 0	6-Jul	Opening & Workshop 1	9:00	9:15	0:15	8:00	3:00	2:00	20:00	17:00			**Opening Remarks**		
	6-Jul		9:15	10:00	0:45	8:15	3:15	2:15	20:15	17:15	WS-1	1060	Innovation to Open New Paradigm for ICAC5/GX/DX	Manabu Tsujimura	Company Executive, Fellow, Ebara, Japan
	6-Jul		10:00	10:45	0:45	9:00	4:00	3:00	21:00	18:00	WS-2	1061	Metallization Challenges in 3D Flash Memory	Masayoshi Tagami	Chief Specialist, Advanced Memory Development Center, KIOXIA, Japan
	6-Jul	Break/Exhibition Hour	10:45	11:15	0:30	9:45	4:45	3:45	21:45	18:45			Break/Exhibition Hour		
	6-Jul	Wrokshop 2	11:15	12:00	0:45	10:15	5:15	4:15	22:15	19:15	WS-3	1062	STT-MRAM technology: applications and scalability challenges	Kangho Lee	Master, Foundry Business, Samsung Electronics, South Korea
	6-Jul	Break/Exhibition Hour	12:00	13:00	1:00	11:00	6:00	5:00	23:00	20:00			Break/Exhibition Hour		
	6-Jul	Workshop 3	13:00	13:45	0:45	12:00	7:00	6:00	0:00	21:00	WS-4	1063	3D Stacking Technologies for Advanced CIS	Yoshihisa Kagawa	Senior Manager, Research Division, Sony Semiconductor Solutions Corporation, Japan
	6-Jul		13:45	14:30	0:45	12:45	7:45	6:45	0:45	21:45	WS-5	1064	NanoBridge Technology for Low-power and Rad-hard AIoT Applications	Munehiro Tada	VP Engineering, NanoBridge Semiconductor, Inc., Japan
	6-Jul	Break/Exhibition Hour	14:30	15:00	0:30	13:30	8:30	7:30	1:30	22:30			Break/Exhibition Hour		
	6-Jul	Workshop 4	15:00	15:45	0:45	14:00	9:00	8:00	2:00	23:00	WS-6	1065	Reliability challenges in advanced interconnects	Olalla Varela Pedreira	R&D Engineer, IMEC, Belgium
	6-Jul		15:45	16:30	0:45	14:45	9:45	8:45	2:45	23:45	WS-7	1066	Extending silicon technology for high-bandwidth optical communications and neuromorphic computing	Bert Jan Offrein	Manager Neuromorphic Devices and Systems, Science& Technology department, IBM research Europe, Switzerland
Day 1	7-Jul	Session 1: Opening/Plenary	8:00	8:15	0:15	7:00	2:00	1:00	19:00	16:00			**Opening Remarks**		
	7-Jul		8:15	8:20	0:05	7:15	2:15	1:15	19:15	16:15			**Award Ceremony**		
	7-Jul		8:20	9:10	0:50	7:20	2:20	1:20	19:20	16:20	S1-1		**Keynote Speech: 3D Heterogeneous Integration for Intelligent Mobile System**	Mitsumasa Koyanagi	Senior Research Fellow, New Industry Creation Hatchery Center, Tohoku University, Japan
	7-Jul		9:10	10:00	0:50	8:10	3:10	2:10	20:10	17:10	S1-2		**Keynote Speech: Foundry Challenges and Opportunities Near the End of Moore's Era**	Gitae Jeong	Corporate EVP, Head of Corporate Office/ Technology Development, Samsung Electronics, South Korea
	7-Jul	Break/Exhibition Hour	10:00	10:30	0:30	9:00	4:00	3:00	21:00	18:00			Break/Exhibition Hour		
	7-Jul	Session 2: Advanced Interconnect	10:30	11:00	0:30	9:30	4:30	3:30	21:30	18:30	S2-1	1073	**Invited Speech: Advanced interconnect challenges beyond 5nm and possible solutions**	Kichul Park{1}, Harsono Simka{2}	{1}Samsung Electronics, Korea; {2}Samsung Semiconductor Inc., United States
	7-Jul		11:00	11:25	0:25	10:00	5:00	4:00	22:00	19:00	S2-2	1018	Advanced Damascene Integration Using Selective Deposition of Barrier Metal with Self Assemble Monolayer	Hiroaki Kawasaki{4}, Mitsuaki Iwashita{4}, Hisashi Warashina{4}, Hiroyuki Nagai{4}, Hiroyuki Komatsu{1}, Yuuki Ozaki{1}, Kazutoshi Iwai{3}, Gyana Pattanaik{2}	{1}JSR Corporation, Japan; {2}TEL Technology Center, America, LLC, United States; {3}Tokyo Electron America, Inc., United States; {4}Tokyo Electron Technology Solutions Ltd., Japan
	7-Jul										S2-3	1029	Low Resistance Subtractive Metal Interconnect Toward Sub 10nm Dimension (*This paper is withdrawn)	He Ren, Hao Jiang, Shi You, Mehul Naik, Alice Lu, Lin Zhou, Chi-I Lang, Wenting Hou, Jianxin Lei, Martin Seamons, Ankit Pokhrel, Praket Jha, Jingmei Liang, Anand Iyer, Chris Lee, Hao Chen, Khoi Phan	Applied Materials, Inc., United States
	7-Jul		11:25	11:50	0:25	10:25	5:25	4:25	22:25	19:25	S2-4	1036	Thermodynamic Evaluation of the Liner and Barrier Properties of a single-Phase Interlayer for Advanced Cu Interconnections	Yuki Yamada, Masataka Yahagi, Junichi Koike	Tohoku University, Japan
	7-Jul		11:50	12:15	0:25	10:50	5:50	4:50	22:50	19:50	S2-5	1053	Selective Barrier for Cu Interconnect Extension in 3nm Node and Beyond	Shi You, He Ren, Mehul Naik, Lu Chen, Feng Chen, Carmen Leal Cervantes, Xiangjin Xie, Keyvan Kashefizadeh	Applied Materials, Inc., United States
	7-Jul	Break	12:15	13:00	0:45	11:15	6:15	5:15	23:15	20:15			Break		
	7-Jul	Exhibitor Presentation 1	13:00	14:00	1:00	12:00	7:00	6:00	0:00	21:00			**Exhibitor Presentation and Guided Virtual Booth Tour 1** TOYO Corporation SCREEN Semiconductor Solutions Co., Ltd. (with booth tour) Moses Lake Industries, Inc. (with booth tour) Merck KGaA (with booth tour)		
	7-Jul	Session 3: 3D and Packaging	14:00	14:30	0:30	13:00	8:00	7:00	1:00	22:00	S3-1	1069	**Invited Speech: Opportunities and challenges brought by 3D-sequential integration**	Perrine Batude	CEA, leti, Minatec, France
	7-Jul		14:30	14:55	0:25	13:30	8:30	7:30	1:30	22:30	S3-2	1003	IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and u- & n- TSVs	Giuliano Sisto{2}, Bilal Chehab{3}, Bertrand Genneret{1}, Rogier Baert{3}, Rongmei Chen{3}, Pieter Weckx{3}, Julien Ryckaert{3}, Richard Chou{1}, Geert Van der Plas{3}, Eric Beyne{3}, Dragomir Milojevic{4}	{1}Cadence Design Systems, United States; {1}Cadence Design Systems, France; {2}Cadence Design Systems / IMEC / École Polytechnique de Bruxelles, United States; {3}IMEC, Belgium; {4}IMEC / École Polytechnique de Bruxelles, Belgium

		JST, KST(UTC+9)			CST, SGT(UTC+8	MSK(UTC+3)	CEST(UTC+2)	Previous day EDT(UTC-4)	PDT(UTC-7)					
		Japan, Korea			China, Taiwan, Singapore	Moscow	Central Europe	USA East Coast	USA Pacific Coast					
Date(JST)	Session #	Start	Finish	Length	Start	Start	Start	Start	Start	Paper #	paper_id	Paper Title	Author Full Names	Organizations
7-Jul		14:55	15:20	0:25	13:55	8:55	7:55	1:55	22:55	S3-3	1007	Fabrication and Characterization of ISC Embedded Interposer for High Performance Interconnection	Won Ji Park, Min Guk Kang, Jae Hee Oh, Shaofeng Ding, Ji Hyung Kim, Je Gwan Hwang, Yunki Choi, Jung Ho Park, Won Hyoung Lee, Seung Ki Nam, Seong Wook Moon, Jongmil Youn, Jeong Hoon Ahn	Samsung Electronics Inc., Korea
7-Jul		15:20	15:45	0:25	14:20	9:20	8:20	2:20	23:20	S3-4	1032	BEoL Damage Evaluation Utilizing Sub Critical Cu-Pillar Shear Tests, Acoustic Emission, nXCT, and SEM/Fib Analysis	Jendrik Silomon{3}, Jürgen Gluch{1}, Juliane Posseckardt{1}, André Clausner{1}, Jens Paul{2}, Dirk Breuer{2}, Ehrenfried Zschech{1}	{1}Fraunhofer IKTS, Germany; {2}GlobalFoundries LLC & Co. KG, Germany; {3}Volkswagen AG, Germany
7-Jul		15:45	16:10	0:25	14:45	9:45	8:45	2:45	23:45	S3-5	1047	Characterization of Low-Temperature Selective Cobalt Atomic Layer Deposition (ALD) for Chip Bonding	Ming-Jui Li{1}, Michael Breeden{2}, Victor Wang{2}, Nyi Myat Khine Linn{3}, Charles Winter{3}, Andrew Kummel{2}, Muhannad Bakir{1}	{1}Georgia Institute of Technology, United States; {2}University of California San Diego, United States; {3}Wayne State University, United States
7-Jul	Break	16:10	16:25	0:15	15:10	10:10	9:10	3:10	0:10			Break		
7-Jul	Poster Session 1	16:25	16:30	0:05	15:25	10:25	9:25	3:25	0:25	PS-1-01	1009	Cu-Cu Bonding Using Optimized Copper Nitride Passivation for 3D Packaging Applications	Haesung Park, Seungmin Park, Yoonho Kim, Sarah Kim	Seoul National University of Science and Technology, Korea
7-Jul		16:30	16:35	0:05	15:30	10:30	9:30	3:30	0:30	PS-1-02	1038	Low Cost TSV Fabrication Technologies Using Anisotropic Si Wet Etching and Conformal Electroless Plating of Barrier and Seed Metals	Tomohiro Shimizu{1}, Shoso Shingubara{1}, Kosuke Matsui{5}, Yuichiro Torinari{5}, Shigeru Watariguchi{2}, Hideki Watanabe{3}, Makoto Motoyoshi{4}	{1}Kansai University, Japan; {2}Meltex Inc., Japan; {3}Meltex.Inc., Japan; {4}Tohoku-MicroTec Co., Ltd., Japan; {5}Tosetsu Inc., Japan
7-Jul		16:35	16:40	0:05	15:35	10:35	9:35	3:35	0:35	PS-1-03	1039	A Thin Adhesive for 3D/2.5D Si Chip Stacking at Low Temperature	Yasuhisa Kayaba, Yuzo Nakamura, Takashi Kozeki, Jun Kamada, Kazuo Kohmura	Mitsui Chemicals, Inc., Japan
7-Jul		16:40	16:45	0:05	15:40	10:40	9:40	3:40	0:40	PS-1-04	1006	An Investigation for Electromagnetic and Electrothermal Coupling Characteristics of Hybrid Bond in Stacked Embedded DRAM with MRPIM	Jingrui Chai{1}, Xiping Jiang{1}, Xudong Gao{1}, Bing Yu{1}, Xiaofeng Zhou{1}, Peng Yin{1}, Song Wang{1}, Jie Tan{1}, Zhengwen Wang{1}, Mei Li{1}, Gang Dong{2}, Qiwei Ren{1}	{1}Xi'an UniIC Semiconductors Co., Ltd., China; {2}Xidian University, China
7-Jul		16:45	16:50	0:05	15:45	10:45	9:45	3:45	0:45	PS-1-05	1033	Copper Large-Scale Grain Growth by UV Nanosecond Pulsed Laser Annealing	Toshiyuki Tabata{2}, Pierre-Edouard Raynal{2}, Fabien Rozé {2}, Sébastien Halty{2}, Louis Thuries{2}, Fuccio Cristiano{1}, Emmanuel Scheid{1}, Fulvio Mazzamuto{2}	{1}LAAS-CNRS, France; {2}Laser Systems & Solutions of Europe, France
7-Jul		16:50	16:55	0:05	15:50	10:50	9:50	3:50	0:50	PS-1-06	1037	Mechanical Properties of Low-K Dielectric Deposited on Subtractively Patterned Cu Lines for Advanced Interconnects	Ivan Ovchinnikov{2}, Askar Rezvanov{3}, Dmitry Seregin{2}, Daniil Abdullaev{2}, Konstantin Vorotilov{2}, Vladimir Gvozdev{1}, Tom Blomberg{5}, Alexey Veselov{5}, Mikhail Baklanov{4}	{1}MERI, Russia; {2}MIREA-Russian Technological University, Russia; {3}Moscow Institute of Physics and Technology, Russia; {4}North China University of Technology, China; {5}Picosun, Finland
7-Jul		16:55	17:00	0:05	15:55	10:55	9:55	3:55	0:55	PS-1-07	1055	The via Resistance Analysis at ALD-to-PVD Tan Transition Layer	Youngsoo Yoon, Changhyun Kim, Junki Jang, Kichang Sung, Hoon Kim, Yunki Choi, Jeong Hoon Ahn, Wonkyu Han, Woojin Jang, Rakhwan Kim, Dongwoo Shin, Juheon Kim, Youngju Lim, Hyunju Yim, Wonmo Kang, Jongmil Youn	Samsung Electronics Inc., Korea
7-Jul		17:00	17:05	0:05	16:00	11:00	10:00	4:00	1:00	PS-1-08	1058	Multi-level Metallization on an Elastomer PDMS for FOWLP-based Flexible Hybrid Electronics	Zhe Wang, Ikumi Ozawa, Yuki Susumago, Tomo Odashima, Noriyuki Takahashi, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima	Tohoku University, Japan
7-Jul		17:05	17:10	0:05	16:05	11:05	10:05	4:05	1:05	PS-1-09	1027	Comparison of Copper and Cobalt Surface Reactivity for Advanced Interconnects	Amine Lakhdari{1}, Mathieu Frégnaux{2}, Louis Caillard{1}, Anne Marie Goncalves{2}, Mikaïlou Thiam{1}, Frédéric Raynal{1}, Arnaud Etcheberry{2}	{1}aveni, France; {2}Université de Versailles Saint-Quentin-en-Yvelines / Institut Lavoisier de Versailles, France
7-Jul										PS-1-10	1043	Grain Structure-Resistivity Relationship of Ru ALD Precursors (*This paper is withdrawn)	Michael Breeden{3}, Victor Wang{3}, Ravindra Kanjolia{1}, Mansour Moinpour{1}, Jacob Woodruff{1}, Harsono Simka{2}, Andrew Kummel{3}	{1}EMD Electronics, a business of Merck KGaA Darmstadt, Germany; {2}Samsung Electronics Inc., United States; {3}University of California San Diego, United States
7-Jul		17:10	17:15	0:05	16:10	11:10	10:10	4:10	1:10	PS-1-11	1056	Fabrication of Highly Doped MLG Patterns Using Selective CVD and MoCl5 Intercalation	Ekkaphop Ketsombun, Tomoki Akimoto, Kazuyoshi Ueno	Shibaura Institute of Technology, Japan
7-Jul		17:15	17:20	0:05	16:15	11:15	10:15	4:15	1:15	PS-1-12	1040	Automated Voids Detection for Metal Filled Trenches with Bottom CD of 10nm	Maryamsadat Hosseini, Gerardo Martinez, Marleen van der Veen, Nicolas Jourdan, Eugenio Dentoni Litta, Naoto Horiguchi	IMEC, Belgium
7-Jul	Poster Session 1: Authors Interview	17:20	17:40	0:20	16:20	11:20	10:20	4:20	1:20			Poster Session 1 - Authors Interview		
7-Jul	Networking Reception	17:50	19:00	1:10	16:50	11:50	10:50	4:50	1:50			Networking Reception		

									Previous day						
			JST, KST(UTC+9)			CST, SGT(UTC+8	MSK(UTC+3)	CEST(UTC+2)	EDT(UTC-4)	PDT(UTC-7)					
			Japan, Korea			China, Taiwan, Singapore	Moscow	Central Europe	USA East Coast	USA Pacific Coast					
	Date(JST)	Session #	Start	Finish	Length	Start	Start	Start	Start	Start	Paper #	paper_id	Paper Title	Author Full Names	Organizations
Day 2	8-Jul	Session 4: Integration	8:00	8:30	0:30	7:00	2:00	1:00	19:00	16:00	S4-1	1075	**Invited Speech: EUV patterning considerations for BEOL scaling**	Nelson Felix	IBM Research, United States
	8-Jul		8:30	9:00	0:30	7:30	2:30	1:30	19:30	16:30	S4-2	1079	**Invited Speech: Holistic method for reducing overlay error at the 5nm node and beyond**	Robert Socha	ASML, United States
	8-Jul		9:00	9:25	0:25	8:00	3:00	2:00	20:00	17:00	S4-3	1015	Advanced Air Gap Formation Scheme Using Volatile Material	Hisashi Warashina{2}, Hiroaki Kawasaki{2}, Hiroyuki Nagai{2}, Nagisa Sato{2}, Tatsuya Yamaguchi{2}, Yuki Kikuchi{1}, Xinghua Sun{1}	{1}TEL Technology Center, America, LLC, United States; {2}Tokyo Electron Technology Solutions Ltd., Japan
	8-Jul		9:25	9:50	0:25	8:25	3:25	2:25	20:25	17:25	S4-4	1048	Process Integration of High Aspect Ratio Vias with a Comparison Between Co and Ru Metallizations	Victor-Hugo Vega-Gonzalez{1}, Daniel Montero{1}, Janko Versluijs{1}, Olalla Varela Pedreira{1}, Nicolas Jourdan{1}, Harinarayanan Puliyalil{1}, Bilal Chehab{1}, Tobias Peissker{2}, Ali Haider{2}, Dmitry Batuk{1}, Gerardo Tadeo Martinez Alanis{1}, Jef Geypen{1}, Quoc Toan{1}	{1}IMEC, Belgium; {2}Lam Research Corporation, United States
	8-Jul		9:50	10:15	0:25	8:50	3:50	2:50	20:50	17:50	S4-5	1054	Advanced 5nm BEOL Integration Development for manufacuring	Jungil Park, Jeong Hoon Ahn, Youngsoo Yoon, Yunki Choi, Junki Jang, Miji Lee	Samsung Electronics Inc., Korea
	8-Jul	Break	10:15	10:30	0:15	9:15	4:15	3:15	21:15	18:15			Break		
	8-Jul	Session 5: Contact/Unit Process	10:30	11:00	0:30	9:30	4:30	3:30	21:30	18:30	S5-1	1074	**Invited Speech: Contact module engineering in advanced CMOS technologies**	Nicolas Breil	Applied Materials, United States
	8-Jul		11:00	11:30	0:30	10:00	5:00	4:00	22:00	19:00	S5-2	1070	**Invited Speech: Intermetallic compounds for Interconnect metal beyond 3 nm node**	Junichi Koike, Toshihiro Kuge, Linghan Chen, Masataka Yahagi	Tohoku University, Japan
	8-Jul		11:30	11:55	0:25	10:30	5:30	4:30	22:30	19:30	S5-3	1031	Contact Interface Characterization of graphene Contacted MoS2 Fets	Vivek Koladi Mootheri{2}, Albert Minj{1}, Goutham Arutchelvan{1}, Alessandra Leonhardt{2}, Inge Asselberghs{1}, Marc Heyns{2}, Iuliana Radu{1}, Dennis Lin{1}	{1}IMEC, Belgium; {2}Katholieke Universiteit Leuven / IMEC, Belgium
	8-Jul		11:55	12:20	0:25	10:55	5:55	4:55	22:55	19:55	S5-4	1034	Metal Wet Recess Challenges and Solutions for Beyond 7nm Fully Aligned via Integration	Corneliu Brown Peethala{1}, Devika Sil{1}, Benjamin Briggs{1}, David Rath{1}, Nick Lanzillo{1}, Kedari Matam{1}, Hosadurga Shobha{1}, K. Choi{1}, Terry Spooner{1}, Donald Canaperi{1}, Minnal Packiam{2}, Dustin Janes{2}, John Casey{2}, L. Chang{2}, Bala Haran{1}	{1}IBM Research, United States; {2}SCREEN SPE USA, LLC DNS Electronics, LLC, United States
	8-Jul		12:20	12:45	0:25	11:20	6:20	5:20	23:20	20:20	S5-5	1057	Improved Contacts to Synthetic Monolayer MoS2 - a Statistical Study	Aravindh Kumar, Alvin Tang, Philip Wong, Krishna Saraswat	Stanford University, United States
	8-Jul	Break	12:45	13:00	0:15	11:45	6:45	5:45	23:45	20:45			Break		
	8-Jul	Exhibitor Presentation 2	13:00	14:00	1:00	12:00	7:00	6:00	0:00	21:00			**Exhibitor Presentation and Guided Virtual Booth Tour 2** Mitsubishi Chemical Corporation TAIYO NIPPON SANSO CORPORATION/RASIRC, Inc.(with booth tour) Tokyo Ohka Kogyo Co.,LTD. (with booth tour) CMC Materials Inc. (with booth tour)		
	8-Jul	Session 6: Memory	14:00	14:30	0:30	13:00	8:00	7:00	1:00	22:00	S6-1	1059	**Invited Speech: Commercialization of MRAM – Historical and Future perspective**	Sumio Ikegawa, Frederick Mancoff, Sanjeev Aggarwal	Everspin Technologies, Inc., United States
	8-Jul		14:30	15:00	0:30	13:30	8:30	7:30	1:30	22:30	S6-2	1072	**Invited Speech: Enabling Ferroelectric Memories in BEOL - towards advanced neuromorphic computing architectures**	David Lehninger, Maximilian Lederer, Tarek Ali, Thomas Kämpfe, Konstantin Mertens, Konrad Seidel	Fraunhofer IPMS/CNT, Germany
	8-Jul		15:00	15:25	0:25	14:00	9:00	8:00	2:00	23:00	S6-3	1008	Controlled ALE-Type Recess of Molybdenum for Future Logic and Memory Applications	Antoine Pacco{1}, Teppei Nakano{3}, Akihisa Iwasaki{2}, Shota Iwahata{3}, Efrain Altamirano Sanchez{1}	{1}IMEC, Belgium; {2}SCREEN Semiconductor Solutions Co., Ltd., Japan; {3}SCREEN SPE Germany GmbH , Germany
	8-Jul		15:25	15:50	0:25	14:25	9:25	8:25	2:25	23:25	S6-4	1028	Multi-Scale Modeling Approach to Assess and mitigiate Wafer Warpage in 3-D NAND Fabrication	Oguzhan Orkut Okudur, Mario Gonzalez, Geert Van Den Bosch, Maarten Rosmeulen	IMEC, Belgium
	8-Jul		15:50	16:15	0:25	14:50	9:50	8:50	2:50	23:50	S6-5	1046	Materials Impact on SRAM Timing: an Ab Initio Study of Interconnects	Shela Aboud{2}, Tue Gunst{1}, Jonathan Cobb{2}, Joanne Huang{2}, Plamen Asenov{2}, Vaida Arcisauskaite{1}	{1}Synopsys Denmark ApS, Belgium; {2}Synopsys Inc., United Kingdom; {2}Synopsys Inc., United States
	8-Jul	Break	16:15	16:25		15:15	10:15	9:15	3:15	0:15			Break		
	8-Jul	Poster Session 2	16:25	16:30	0:05	15:25	10:25	9:25	3:25	0:25	PS-2-01	1044	A Method of chemical-Mechanical Polishing of a Thick Silver Layer on Patterned Silicon Wafer	Evgeny Danilkin{2}, Valentina Gaydeday{2}, Jose Valdez{2}, Vladimir Krupnik{2}, Igor Ivanov{1}, Sergey Ermakov{3}, Daria Navolotskaya{3}	{1}AxBio inc., United States; {2}Crocus Nano Electronics, Russia; {3}Saint Petersburg State University, Russia
	8-Jul		16:30	16:35	0:05	15:30	10:30	9:30	3:30	0:30	PS-2-02	1051	Atomic Layer Deposition of Titanium Silicate for Multi-Patterning Process	Sanghun Lee{3}, Seunggi Seo{3}, Wonate Noh{1}, Il-Kwon Oh{2}, Hyungjun Kim{3}	{1}Air Liquide Laboratory Korea, Korea; {2}Ajou University, Korea; {3}Yonsei University, Korea
	8-Jul		16:35	16:40	0:05	15:35	10:35	9:35	3:35	0:35	PS-2-03	1022	Microstructural Optimization of Tungsten for Low Resistivity Using Ion Beam Deposition	Frank Cerio, Rutvik Mehta, Paul Turner, Robert Caldwell, Jinho Kim	Veeco Instruments Inc., United States

		Previous day												
		JST, KST(UTC+9)			CST, SGT(UTC+8	MSK(UTC+3)	CEST(UTC+2)	EDT(UTC-4)	PDT(UTC-7)					
		Japan, Korea			China, Taiwan, Singapore	Moscow	Central Europe	USA East Coast	USA Pacific Coast					
Date(JST)	Session #	Start	Finish	Length	Start	Start	Start	Start	Start	Paper #	paper_id	Paper Title	Author Full Names	Organizations
8-Jul		16:40	16:45	0:05	15:40	10:40	9:40	3:40	0:40	PS-2-04	1030	An Alternative to Tungsten in 3D-NAND Technology	Dominique Suhr, Vincent Mevellec, Mikaïlou Thiam, Jonathan Idier, Frédéric Raynal, Hermine Berthon, Elisa Perrault, Nicolas Hann, Céline Doussot, Yeeseul Kim, Mathilde Baus, Amine Lakhdari, Gaëlle Guittet, Louis Caillard	aveni, France
8-Jul		16:45	16:50	0:05	15:45	10:45	9:45	3:45	0:45	PS-2-05	1021	Atomic Layer Deposition of RuO2 Using a New metalorganic Precursor As a Diffusion Barrier for Ru Interconnect	Youn-Hye Kim{3}, Yohei Kotsugi{2}, Taehoon Cheon{1}, Rahul Ramesh{3}, Soo-Hyun Kim{3}	{1}Daegu Gyeongbuk Institute of Science and Technology, Korea; {2}Tanaka Precious Metals, Korea; {3}Yeungnam University, Korea
8-Jul		16:50	16:55	0:05	15:50	10:50	9:50	3:50	0:50	PS-2-06	1024	An All-Wet, Low Cost RDL Fabrication Process with Electroless Plated Seed/Barrier Layers	Ziru Cai, Yingtao Ding, Zhaohu Wu, Ziyue Zhang, Yuwen Su, Zhiming Chen	Beijing Institute of Technology, China
8-Jul		16:55	17:00	0:05	15:55	10:55	9:55	3:55	0:55	PS-2-07	1049	Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition on Silicon	Cheng-Hsuan Kuo{3}, Victor Wang{3}, Zichen Zhang{3}, Seonguk Yun{3}, Jeffrey Spiegelman{1}, Daniel Alvarez{1}, Harsono Simka{2}, Andrew Kummel{3}	{1}RASIRC, United States; {2}Samsung Electronics Inc., United States; {3}University of California San Diego, United States
8-Jul		17:00	17:05	0:05	16:00	11:00	10:00	4:00	1:00	PS-2-08	1050	Impact of Nanosecond Laser Anneal on PVD Ru Films	Devika Sil{1}, Yasir Sulehria{1}, Oleg Gluschenkov{1}, Takeshi Nogami{1}, Roger Cornell{1}, Andrew Simon{1}, Juntao Li{1}, James Demarest{1}, Bala Haran{1}, Christian Lavoie{1}, Jean L Jordan-Sweet{1}, V. Stanic{1}, Junjun Liu{3}, Karim Huet{2}, Fulvio Mazzamuto{2}	{1}IBM Research, United States; {2}Laser Systems & Solutions of Europe, France; {3}SCREEN SPE USA, LLC, United States
8-Jul		17:05	17:10	0:05	16:05	11:05	10:05	4:05	1:05	PS-2-09	1052	Development of Manganese Nitride Resistor with Near-Zero Temperature-Coefficient of Resistance to Achieve High-Thermal-Stability ICs	Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka	Tohoku University, Japan
8-Jul		17:10	17:15	0:05	16:10	11:10	10:10	4:10	1:10	PS-2-10	1013	Design of an Integrated III-V on Silicon Semiconductor Laser for Spiking Neural Networks	Keshia Mekemeza Ona, Benoit Charbonnier, Karim Hassan	CEA-Leti, Université Grenoble Alpes, F-38000 Grenoble, France
8-Jul		17:15	17:20	0:05	16:15	11:15	10:15	4:15	1:15	PS-2-11	1042	Virtual Metrology Equipped with a Variability Analyzer in Chemical Mechanical Polishing	Lingyen Yeh, Shu Chun Huang	Sun Innovation Co., Ltd., Taiwan
8-Jul		17:20	17:25	0:05	16:20	11:20	10:20	4:20	1:20	PS-2-12	1010	Interconnects Variability Control for High Voltage Applications	Kwang Sing Yew, Yi Jiang, Wanbing Yi, Ramasamy Chockalingam, Ran Xing Ong, Bo Li, Juan Boon Tan	GlobalFoundries, Singapore
8-Jul		17:25	17:30	0:05	16:25	11:25	10:25	4:25	1:25	PS-2-13	1019	A Study on the nitridation of Barrier Liner Contribution to Galvanic Corrosion of Copper bondpad	Xiaodong Li, Ramasamy Chockalingam, Poh Chuan Ang, Wah Peng Neo, Juan Boon Tan	GlobalFoundries, Singapore
8-Jul	Poster Session 2: Authors Interview	17:30	17:45	0:15	16:30	11:30	10:30	4:30	1:30			Poster Session 2 - Authors Interview		
Day 3														
9-Jul	Session 7: Advanced Interconnect	8:00	8:30	0:30	7:00	2:00	1:00	19:00	16:00	S7-1	1080	**Invited Speech: EM performance improvements for Cu interconnects with Ru-based liner and Co cap in advanced nodes**	Koichi Motoyama	IBM Research, United States
9-Jul		8:30	8:55	0:25	7:30	2:30	1:30	19:30	16:30	S7-2	1012	XPS Diffusion Analysis of Ta(N)/Ru Diffusion Barriers for Cobalt Interconnects	Bettina Wehring, Lukas Gerlich, Benjamin Uhlig	Fraunhofer IPMS, Germany
9-Jul		8:55	9:20	0:25	7:55	2:55	1:55	19:55	16:55	S7-3	1014	Exploring W-Cu Hybrid Dual Damascene metallization for Future Nodes	Marleen van der Veen{3}, Olalla Varela Pedreira{3}, Nancy Heylen{3}, Nicolas Jourdan{3}, Stéphane Larivière{3}, Seongho Park{3}, Herbert Struyf{3}, Zsolt Tőkei{3}, Wei Lei{2}, Shiris Pethe{2}, Shinjae Hwang{2}, Feng Chen{2}, Zhiyan Wu{2}, Jérôme Machillot{1}, Andrew Cockburn{1}, A. Jansen{2}	{1}Applied Materials Belgium, Belgium; {2}Applied Materials, Inc., United States; {3}IMEC, Belgium
9-Jul		9:20	9:45	0:25	8:20	3:20	2:20	20:20	17:20	S7-4	1017	Selective Deposition of AlOx for Fully Aligned via in Nano Cu Interconnects	Son Van Nguyen{1}, Hosadurga Shobha{1}, Corneliu Brown Peethala{1}, Thomas Haigh{1}, Huai Huang{1}, Juntao Li{1}, James Demarest{1}, Balasubramanian Pranatharthi Haran{1}, Dennis Hausmann{2}, Paul Lemaire{2}, Kashish Sharma{2}, Pankaj Ramani{2}, Arpan Mahorowala{2}	{1}IBM Research, United States; {2}Lam Research Corporation, United States
9-Jul		9:45	10:10	0:25	8:45	3:45	2:45	20:45	17:45	S7-5	1026	Aluminide Intermetallics for Advanced Interconnect metallization: Thin Film Studies	Jean-Philippe Soulié, Zsolt Tőkei, Johan Swerts, Christoph Adelmann	IMEC, Belgium
9-Jul	Next Conference Announcement/Break	10:10	10:30	0:20	9:10	4:10	3:10	21:10	18:10			**Next Conference Announcement**		

		JST, KST(UTC+9)			CST, SGT(UTC+8	MSK(UTC+3)	CEST(UTC+2)	Previous day EDT(UTC-4)	PDT(UTC-7)					
		Japan, Korea			China, Taiwan, Singapore	Moscow	Central Europe	USA East Coast	USA Pacific Coast					
Date(JST)	Session #	Start	Finish	Length	Start	Start	Start	Start	Start	Paper #	paper_id	Paper Title	Author Full Names	Organizations
9-Jul	Session 8: RC Scaling/Reliability	10:30	11:00	0:30	9:30	4:30	3:30	21:30	18:30	S8-1	1076	**Invited Speech: On-die interconnect technologies for future technology nodes**	Mauro Kobrinsky	Intel, United States
9-Jul		11:00	11:30	0:30	10:00	5:00	4:00	22:00	19:00	S8-2	1071	**Invited Speech: Reliability Characterization on Advanced FinFET Technology**	Kihyun Choi, Taeyoung Jeong, Jinju Kim, Seungjin Choo, Younghan Kim, Myungsoo Yeo, Miji Lee, Jinseok Kim, Euncheol Lee	Samsung Electronics, Korea
9-Jul		11:30	11:55	0:25	10:30	5:30	4:30	22:30	19:30	S8-3	1016	Reliability of Barrierless PVD Mo	Davide Tierno, Maryamsadat Hosseini, Marleen van der Veen, Anish Dagol, Kristof Croes, Steven Demuynck, Zsolt Tőkei, Eugenio Dentoni Litta, Naoto Horiguchi	IMEC, Belgium
9-Jul		11:55	12:20	0:25	10:55	5:55	4:55	22:55	19:55	S8-4	1025	Joule Heating Investigation for Advanced Interconnect Schemes with airgaps	Melina Lofrano, Olalla Varela Pedreira, Ivan Ciofi, Herman Oprins, Seongho Park Park, Zsolt Tőkei	IMEC, Belgium
9-Jul		12:20	12:45	0:25	11:20	6:20	5:20	23:20	20:20	S8-5	1035	Effects of Composition Deviation of $CuAl_2$ on BTS and TDDB Reliability	Toshihiro Kuge, Masataka Yahagi, Junichi Koike	Tohoku University, Japan
9-Jul	Next Conference Announcement	12:45	12:50	0:05	11:45	6:45	5:45	23:45	20:45			**Next Conference Announcement**		
9-Jul	Break	12:50	13:00	0:10	11:50	6:50	5:50	23:50	20:50			Break		
9-Jul	Exhibitor Presentation 3	13:00	14:00	1:00	12:00	7:00	6:00	0:00	21:00			**Exhibitor Presentation and Guided Virtual Booth Tour 3** Tower Partners Semiconductor Co., Ltd TOKYO ELECTRON LIMITED APOLLOWAVE Corporation (with booth tour) EBARA CORPORATION (with booth tour) Showa Denko Materials Co., Ltd. (with booth tour)		
9-Jul	Session 9: DTCO/Novel System	14:00	14:30	0:30	13:00	8:00	7:00	1:00	22:00	S9-1	1077	**Invited Speech: Technological Influences in Designing and Building a Wafer Scale Interconnect**	Gary Lauterback	Cerebras Systems, United States
9-Jul		14:30	15:00	0:30	13:30	8:30	7:30	1:30	22:30	S9-2	1078	**Invited Speech: Resistive memories for neuromorphic hardware**	Elisa Vianello	CEA-Leti, France
9-Jul		15:00	15:25	0:25	14:00	9:00	8:00	2:00	23:00	S9-3	1020	Advanced CMP Process Control by Using Machine Learning Image Analysis	Min-Hsuan Hsu, Chih-Chen Lin, Hsiang-Meng Yu, Kuang-Wei Chen, Tuung Luoh, Ling-Wuu Yang, Ta-Hone Yang, Kuang-Chao Chen	Macronix International Co. Ltd., Technology Development Center, Taiwan
9-Jul		15:25	15:50	0:25	14:25	9:25	8:25	2:25	23:25	S9-4	1041	Two-Level MOL and VHV Routing Style to Enable Extreme Height Scaling Beyond 2nm Technology Node	Bilal Chehab, Odysseas Zografos, Eugenio Dentoni Litta, Zubair Ahmed, Pieter Schuddinck, Doyoung Jang, Geert Hellings, Alessio Spessot, Pieter Weckx, Julien Ryckaert	IMEC, Belgium
9-Jul		15:50	16:15	0:25	14:50	9:50	8:50	2:50	23:50	S9-5	1045	Novel IR/EM-Aware Power Grid Design and Analysis Methodologies for Optimal PPA at Sub-10nm Technology Nodes	Grant Miller, Saurabh Jain, Santosh Kelgeri, Pranav Raganathan, Ahmet Ceyhan	Advanced Design, United States
9-Jul	Closing Remarks	16:15	16:20	0:05	15:15	10:15	9:15	3:15	0:15					