### IEEE International Interconnect Technology Conference (IITC) 2021
#### Program At-a-Glance

<table>
<thead>
<tr>
<th></th>
<th>Day 0</th>
<th>Day 1</th>
<th>Day 2</th>
<th>Day 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>July 6</strong></td>
<td>IITC Workshop</td>
<td>IITC Regular Sessions</td>
<td>IITC Regular Sessions</td>
<td>IITC Regular Sessions</td>
</tr>
<tr>
<td><strong>Morning 1</strong></td>
<td></td>
<td>8:00-10:00 Opening Remarks/</td>
<td>8:00-10:15 Integration</td>
<td>8:00-10:15 Advanced Interconnect</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Award Ceremony/Plenary</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Morning 2</strong></td>
<td></td>
<td>10:30-12:40 Advanced Interconnect</td>
<td>10:30-12:45 Contact/Unit Process</td>
<td>10:30-12:50 RC Scaling/Reliability</td>
</tr>
<tr>
<td>Lunch time</td>
<td>12:00-13:00</td>
<td>13:00-14:00 Exhibitor Presentation/ Booth Tour</td>
<td>13:00-14:00 Exhibitor Presentation/ Booth Tour</td>
<td>13:00-14:00 Exhibitor Presentation/ Booth Tour</td>
</tr>
<tr>
<td>Afternoon 1</td>
<td>13:00-16:30 Workshop</td>
<td>14:00-16:10 3D and Packaging</td>
<td>14:00-16:15 Memory</td>
<td>14:00-16:20 DTCO/Novel System Closing Remarks</td>
</tr>
<tr>
<td>Afternoon 2</td>
<td></td>
<td>16:25-17:40 Poster Session Short Presentation and Authors’ interview</td>
<td>16:25-17:45 Poster Session Short Presentation and Authors’ interview</td>
<td></td>
</tr>
<tr>
<td>Evening</td>
<td></td>
<td>17:50-19:00 Networking Reception</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
IEEE International Interconnect Technology Conference (IITC) 2021
Program Schedule

Tuesday, July 6, 2021
9:00 am – 4:30 pm  Workshop
Session Chairs:

9:00 am - 9:15 am
Opening Remarks

9:15 am - 10:00 am
WS-1. Innovation to Open New Paradigm for ICAC5/GX/DX
Manabu Tsujimura
Company Executive, Fellow, Ebara

10:00 am - 10:45 am
WS-2. Metallization Challenges in 3D Flash Memory
Masayoshi Tagami
KIOXIA

10:45 am - 11:15 am
Break/Exhibition Hour

11:15 am - 12:00 pm
WS-3. STT-MRAM technology: applications and scalability challenges
Kangho Lee
Master, Foundry Business, Samsung Electronics, South Korea

12:00 pm - 1:00 pm
Break/Exhibition Hour

1:00 pm - 1:45 pm
WS-4. 3D Stacking Technologies for Advanced CIS
Yoshihisa Kagawa
Senior Manager, Research Division, Sony Semiconductor Solutions Corporation, Japan

1:45 pm - 2:30 pm
WS-5. NanoBridge Technology for Low-power and Rad-hard AIoT Applications
Munehiro Tada
VP Engineering, NanoBridge Semiconductor, Inc.
2:30 pm - 3:00 pm
Break/Exhibition Hour

3:00 pm - 3:45 pm
WS-6. Reliability challenges in advanced interconnects
Olalla Varela Pedreira
R&D Engineer, IMEC, Belgium

3:45 pm - 4:30 pm
WS-7. Extending silicon technology for high-bandwidth optical communications and neuromorphic computing
Bert Jan Offrein
Manager Neuromorphic Devices and Systems, Science& Technology department, IBM research Europe, Switzerland
**Wednesday, July 7, 2021**

**8:00 am – 10:00 am  Session 1: Opening/Plenary**

Session Chairs:

8:00 am - 8:15 am  
**Opening Remarks**

8:15 am - 8:20 am  
**Award Ceremony**

8:20 am - 9:10 am  
**S1-1. Keynote Speech: 3D Heterogeneous Integration for Intelligent Mobile System**

Prof. Mitsumasa Koyanagi  
Senior Research Fellow, New Industry Creation Hatchery Center, Tohoku University, Japan

9:10 am - 10:00 am  
**S1-2. Keynote Speech: Foundry Challenges and Opportunities Near the End of Moore’s Era**

Dr. Gitee Jeong  
Corporate EVP, Head of Corporate Office/ Technology Development, Samsung Electronics, South Korea

10:00 am - 10:30 am  
**Break/Exhibition Hour**

**Wednesday, July 7, 2021**

**10:30 am – 12:40 pm  Session 2: Advanced Interconnect**

10:30 am - 11:00 am  
**S2-1. Invited Speech: Advanced interconnect challenges beyond 5nm and possible solutions**

KC(Kichul) Park  
Samsung Electronics, South Korea

11:00 am - 11:25 am  
**S2-2. Advanced Damascene Integration Using Selective Deposition of Barrier Metal with Self Assemble Monolayer**

Hiroaki Kawasaki{4}, Mitsuaki Iwashita{4}, Hisashi Warashina{4}, Hiroyuki Nagai{4}, Hiroyuki Komatsu{1}, Yuuki Ozaki{1}, Kazutoshi Iwai{3}, Gyana Pattanaik{2}  
{1}JSR corporation, Japan; {2}TEL Technology Center, America, LLC, United States; {3}Tokyo Electron America, Inc., United States; {4}Tokyo Electron Limited, Japan
11:25 am - 11:50 am
S2-3. Low Resistance Subtractive Metal Interconnect Toward Sub 10nm Dimension
He Ren, Hao Jiang, Shi You, Mehul Naik, Alice Lu, Lin Zhou, Chi-I Lang, Wenting Hou, Jianxin Lei, Martin Seamons, Ankit Pokhrel, Prakte Jha, Jingmei Liang
Applied Materials, United States

11:50 am - 12:15 pm
S2-4. Thermodynamic Evaluation of the Liner and Barrier Properties of a single-Phase Interlayer for Advanced Cu Interconnections
Yuki Yamada, Masataka Yahagi, Junichi Koike
Tohoku University, Japan

12:15 pm - 12:40 pm
S2-5. Selective Barrier for Cu Interconnect Extension in 3nm Node and Beyond
Shi You, He Ren, Mehul Naik, Lu Chen, Feng Chen, Carmen Leal Cervantes, Xiangjin Xie, Keyvan Kashefizadeh
Applied Materials, Inc., United States

12:40 pm - 1:00 pm
Break

1:00 pm - 2:00 pm
Exhibitor Presentation 1

Wednesday, July 7, 2021
2:00 pm – 4:10 pm Session 3: 3D and Packaging
Session Chairs:

2:00 pm - 2:30 pm
S3-1. Invited Speech: Opportunities and challenges brought by 3D-sequential integration
Dr. Perrine Batude
Senior scientist and project manager, CEA-Leti, France

2:30 pm - 2:55 pm
S3-2. IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and u- & n- TSVs
Giuliano Sisto{2}, Bilal Chehab{3}, Bertrand Genneret{1}, Rogier Baert{3}, Rongmei Chen{3}, Pieter Weckx{3}, Julien Ryckaert{3}, Richard Chou{1}, Geert Van der Plas{3}, Eric Beyne{3}, Dragomir Milojovic{3}
{1}CADENCE, United States; {1}CADENCE, France; {2}Cadence Design Systems, United States; {3}IMEC, Belgium
2:55 pm - 3:20 pm
S3-3. Fabrication and Characterization of ISC Embedded Interposer for High Performance Interconnection
Won Ji Park, Min Guk Kang, Jae Hee Oh, Shaofeng Ding, Ji Hyung Kim, Je Gwan Hwang, Yun Ki Choi, Jung Ho Park, Won Hyoung Lee, Seung Ki Nam, Seong Wook Moon, Jong Mil Youn, Jeong Hoon Ahn
Samsung Electronics, South Korea

3:20 pm - 3:45 pm
S3-4. BEoL Damage Evaluation Utilizing Sub Critical Cu-Pillar Shear Tests, Acoustic Emission, nXCT, and SEM/Fib Analysis
Jendrik Silomon{3}, Jürgen Gluch{1}, Juliane Posseckardt{1}, André Clausner{1}, Jens Paul{2}, Dirk Breuer{2}, Ehrenfried Zschech{1}
{1}Fraunhofer IKTS, Germany; {2}Globalfoundries LLC & Co. KG, Germany; {3}Volkswagen AG, Germany

3:45 pm - 4:10 pm
S3-5. Characterization of Low-Temperature Selective Cobalt Atomic Layer Deposition (ALD) for Chip Bonding
Ming-Jui Li{3}, Michael Breeden{1}, Victor Wang{1}, Nyi Myat Khine Linn{2}, Charles Winter{2}, Andrew Kummel{1}, Muhannad Bakir{3}
{1}Chemistry and Biochemistry Department, University of California San Diego, United States; {2}Chemistry Department, Wayne State University, United States; {3}Electrical and Computer Engineering Department, Georgia Institute of Technology, United States

4:10 pm - 4:25 pm
Break

Wednesday, July 7, 2021
4:25 pm – 5:40 pm Poster Session 1
Session Chairs:

4:25 pm - 4:30 pm
PS-1-01. Cu-Cu Bonding Using Optimized Copper Nitride Passivation for 3D Packaging Applications
Haesung Park, Seungmin Park, Yoonho Kim, Sarah Kim
Seoul National University of Science & Technology, South Korea
4:30 pm - 4:35 pm
**PS-1-02. Low Cost TSV Fabrication Technologies Using Anisotropic Si Wet Etching and Conformal Electrolest Plating of Barrier and Seed Metals**
Tomohiro Shimizu{1}, Shoso Shingubara{1}, Kosuke Matsui{5}, Yuichiro Torinari{5}, Shigeru Watariguchi{2}, Hideki Watanabe{3}, Makoto Motoyoshi{4}
{1}Kansai University, Japan; {2}Meltex Inc., Japan; {3}Meltex Inc., Japan; {4}Tohoku-Microtec, Japan; {5}Tosetsu Inc., Japan

4:35 pm - 4:40 pm
**PS-1-03. A Thin Adhesive for 3D/2.5D Si Chip Stacking at Low Temperature**
Yuzo Nakamura, Takashi Kozeki, Jun Kamada, Kazuo Kohmura
Mitsui Chemicals, Inc., Japan

4:40 pm - 4:45 pm
**PS-1-04. An Investigation for Electromagnetic and Electrothermal Coupling Characteristics of Hybrid Bond in Stacked Embedded DRAM with MRPII**
Jingrui Chai{1}, Xiping Jiang{1}, Xudong Gao{1}, Bing Yu{1}, Xiaofeng Zhou{1}, Peng Yin{1}, Song Wang{1}, Jie Tan{1}, Zhengwen Wang{1}, Gang Dong{2}, Qiwei Ren{1}
{1}Xi'an UniIC Semiconductors, China; {2}Xidian University, China

4:45 pm - 4:50 pm
**PS-1-05. Copper Large-Scale Grain Growth by UV Nanosecond Pulsed Laser Annealing**
Toshiyuki Tabata{2}, Pierre-Edouard Rayna{2}, Fabien Roz{2}, Sébastien Halty{2}, Louis Thuries{2}, Fuccio Cristiano{1}, Emmanuel Scheid{1}, Fulvio Mazzamuto{2}
{1}LAAS-CNRS, France; {2}Laser Systems & Solutions of Europe (LASSE), France

4:50 pm - 4:55 pm
**PS-1-06. Mechanical Properties of Low-K Dielectric Deposited on Subtractively Patterned Cu Lines for Advanced Interconnects**
Ivan Ovchinnikov{3}, Askar Rezvanov{2}, Dmitry Seregin{3}, Daniil Abdullaev{3}, Konstantin Vorotilov{3}, Vladimir Gvozdev{1}, Tom Blomberg{5}, Alexey Veselov{5}, Mikhail Baklanov{4}
{1}MERI, Russia; {2}MIPT, MERI, Russia; {3}MIREA-Russian Technological University, Russia; {4}NCUT, China; {5}Picosun, Finland

4:55 pm - 5:00 pm
**PS-1-07. The via Resistance Analysis at ALD-to-PVD Tan Transition Layer**
Changhyun Kim, Junki Cang, Kichang Sung, Hoon Kim, Yunki Choi, Jeonghoon Ahn, Wonkyu Han, Woojin Jang, Rakhwan Kim, Juheon Kim, Youngju Lim, Hyunju Yim, Wonmo Kang
Samsung Electronics Inc., South Korea
5:00 pm - 5:05 pm
**PS-1-08. Multi-level Metallization on an Elastomer PDMS for FOWLP-based Flexible Hybrid Electronics**
Zhe Wang, Ikumi Ozawa, Yuki Susumago, Tomo Odashima, Noriyuki Takahashi, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima
Tohoku University, Japan

5:05 pm - 5:10 pm
**PS-1-09. Comparison of Copper and Cobalt Surface Reactivity for Advanced Interconnects**
Amine Lakhdari{1}, Mathieu Frégnaux{2}, Louis Caillard{1}, Anne Marie Goncalves{2}, Mikaïlou Thiam{1}, Frédéric Raynal{1}, Arnaud Etcheberry{2}
{1}aveni, France; {2}Institut Lavoisier de Versailles, France

5:10 pm - 5:15 pm
**PS-1-10. Grain Structure-Resistivity Relationship of Ru ALD Precursors**
Michael Breeden{3}, Victor Wang{3}, Ravindra Kanjolia{1}, Mansour Moinpour{1}, Jacob Woodruff{1}, Harsono Simka{2}, Andrew Kummel{3}
{1}Merck KGaA, Darmstadt, Germany; {2}Samsung, United States; {3}UC San Diego, United States

5:15 pm - 5:20 pm
**PS-1-11. Fabrication of Highly Doped MLG Patterns Using Selective CVD and MoCl5 Intercalation**
Ekkaphop Ketsombun, Tomoki Akimoto, Kazuyoshi Ueno
Shibaura Institute of Technology, Japan

5:20 pm - 5:25 pm
**PS-1-12. Automated Voids Detection for Metal Filled Trenches with Bottom CD of 10nm**
Maryamsadat Hosseini, Gerardo Martinez, Maarleen van der Veen, Nicolas Jourdan, Eugenio Dentoni Litta, Naoto Horiguchi
imec, Belgium

5:25 pm - 5:40 pm
**Poster Session 1 - Authors Interview**

5:50 pm - 7:00 pm
**Networking Reception**
Thursday, July 8, 2021
8:00 am – 10:15 am  Session 4: Integration
Session Chairs:

8:00 am - 8:30 am
S4-1. Invited Speech: EUV patterning considerations for BEOL scaling
Nelson Felix
Director, Process Technology, IBM Research, USA

8:30 am - 9:00 am
S4-2. Invited Speech: Analysis of edge placement error (EPE) at the 5nm node and beyond
Robert Socha
Fellow, ASML Brion

9:00 am - 9:25 am
S4-3. Advanced Air Gap Formation Scheme Using Volatile Material
Hisashi Warashina{2}, Hiroaki Kawasaki{2}, Hiroyuki Nagai{2}, Nagisa Sato{2}, Tatsuya Yamaguchi{3}, Yuki Kikuchi{1}, Xinghua Sun{1}
{1}TEL TECHNOLOGY CENTER, AMERICA, LLC, United States; {2}TOKYO ELECTRON LIMITED, Japan; {3}TOKYO ELECTRON TECHNOLOGY SOLUTIONS LIMITED, Japan

9:25 am - 9:50 am
S4-4. Process Integration of High Aspect Ratio Vias with a Comparison Between Co and Ru Metallizations
Victor-Hugo Vega-Gonzalez{1}, Daniel Montero{1}, Janko Versluijs{1}, Olalla Varela Pedreira{1}, Nicolas Jourdan{1}, Harinarayanan Puliyalil{1}, Bilal Chehab{1}, Tobias Peissker{2}, Ali Haider{2}, Dmitry Batuk{1}, Gerardo Tadeo Martinez Alanis{1}, Jef Geyp
{1}IMEC, Belgium; {2}LAM, United States

9:50 am - 10:15 am
S4-5. Advanced 5nm BEOL Integration Development for manufacturing
Jungil Park, Jeong Hoon Ahn, Youngsoo Yoon, Yunki Choi, Junki Jang, Miji Lee
Samsung electronics, South Korea

10:15 am - 10:30 am
Break
Thursday, July 8, 2021
10:30 am – 12:45 pm  Session 5: Contact/Unit Process

Session Chairs:

10:30 am - 11:00 am  
**S5-1. Invited Speech: Contact module progress and challenges in advanced CMOS technologies**
Nicolas Breil
Applied Materials, USA

11:00 am - 11:30 am  
**S5-2. Invited Speech: Intermetallic compounds for Interconnect metal beyond 3 nm node**
Prof. Junichi Koike
Professor, Dept. of Materials Science, Tohoku University, Japan

11:30 am - 11:55 am  
**S5-3. Contact Interface Characterization of graphene Contacted MoS2 Fets**
Vivek Koladi Mootheri{2}, Albert Minj{1}, Goutham Arutchelvan{1}, Alessandra Leonhardt{2}, Inge Asselberghs{1}, Marc Heyns{2}, Iuliana Radu{1}, Dennis Lin{1}
{1}IMEC, Belgium; {2}KU Leuven/IMEC, Belgium

11:55 am - 12:20 pm  
**S5-4. Metal Wet Recess Challenges and Solutions for Beyond 7nm Fully Aligned via Integration**
Brown Peethala{1}, Devika Sil{1}, Benjamin Briggs{1}, David Rath{1}, Nick Lanzillo{1}, Kedari Matam{1}, Shobha Hosadurga{1}, Terry Spooner{1}, Donald Canaperi{1}, Minnal Packiam{2}, Dustin Janes{2}, John Casey{2}
{1}IBM Research, United States; {2}Screen, Albany, United States

12:20 pm - 12:45 pm  
**S5-5. Improved Contacts to Synthetic Monolayer MoS2 - a Statistical Study**
Aravindh Kumar, Alvin Tang, Philip Wong, Krishna Saraswat
Stanford University, United States

12:45 pm - 1:00 pm  
**Break**

1:00 pm - 2:00 pm  
**Exhibitor Presentation 2**
Thursday, July 8, 2021
2:00 pm – 4:15 pm  Session 6: Memory
Session Chairs:

2:00 pm - 2:30 pm
S6-1. Invited Speech: Commercialization of MRAM – Historical and Future perspective
Dr. Sumio Ikegawa
Distinguished Member of the Technical Staff in Technology R&D Department, Everspin Technologies Inc., USA

2:30 pm - 3:00 pm
S6-2. Invited Speech: Enabling Ferroelectric Memories in BEOL - towards advanced neuromorphic computing architectures
Mr. David Lehninger
Project manager, Fraunhofer Center for Nanoelectronic Materials, Fraunhofer, Germany

3:00 pm - 3:25 pm
S6-3. Controlled ALE-Type Recess of Molybdenum for Future Logic and Memory Applications
Antoine Pacco{1}, Teppei Nakano{2}, Akihisa Iwasaki{2}, Shota Iwahata{3}, Efrain Altamirano Sanchez{1}
{1}imec, Belgium; {2} SCREEN, Germany; {3}SCREEN, Japan

3:25 pm - 3:50 pm
S6-4. Multi-Scale Modeling Approach to Assess and mitigate Wafer Warpage in 3-D NAND Fabrication
Oguzhan Orkut Okudur, Mario Gonzalez, Geert Van Den Bosch, Maarten Rosmeulen
imec, Belgium

3:50 pm - 4:15 pm
S6-5. Materials Impact on SRAM Timing: an Ab Initio Study of Interconnects
Shela Aboud, Tue Gunst, Jonathan Cobb, Joanne Huang, Plamen Asenov, Vaida Arcisauskaite
Synopsys, United States; Synopsys, Belgium; Synopsys, United Kingdom

4:15 pm - 4:25 pm
Break
Thursday, July 8, 2021
4:25 pm – 5:45 pm  Poster Session 2

Session Chairs:

4:25 pm - 4:30 pm
PS-2-01. A Method of chemical-Mechanical Polishing of a Thick Silver Layer on Patterned Silicon Wafer
Evgeny Danilkin{2}, Valentina Gaydeday{2}, Jose Valdez{2}, Vladimir Krupnik{2}, Igor Ivanov{1}, Sergey Ermakov{3}, Daria Navolotskaya{3}
{1}AxBio inc., United States; {2}Crocus Nano Electronics, Russia; {3}Saint Ptetersburg State University, Russia

4:30 pm - 4:35 pm
PS-2-02. Atomic Layer Deposition of Titanium Silicate for Multi-Patterning Process
Sanghun Lee{3}, Seunggi Seo{3}, Wonate Noh{1}, Il-Kwon Oh{2}, Hyungjun Kim{3}
{1}Air Liquide Laboratory Korea, South Korea; {2}Ajou University, South Korea; {3}Yonsei University, South Korea

4:35 pm - 4:40 pm
PS-2-03. Microstructural Optimization of Tungsten for Low Resistivity Using Ion Beam Deposition
Frank Cerio{1}, Rutvik Mehta{1}, Paul Turner{2}, Robert Caldwell{1}, Jinho Kim{1}
{1}Veeco Instruments Inc, United States; {2}Veeco Instruments Inc., United States

4:40 pm - 4:45 pm
PS-2-04. An Alternative to Tungsten in 3D-NAND Technology
Dominique Suhr, Vincent Mevelle, Mikailou Thiam, Jonathan Idier, Frédéric Raynal, Hermine Berthon, Elisa Perrault, Nicolas Hann, Céline Doussot, Yeeseul Kim, Mathilde Baus, Amine Lakhdiri, Gaëlle Guittet
Aveni, France

4:45 pm - 4:50 pm
PS-2-05. Atomic Layer Deposition of RuO2 Using a New metalorganic Precursor As a Diffusion Barrier for Ru Interconnect
Youn-Hye Kim{3}, Yohei Kotsugi{2}, Taehoon Cheon{1}, Rahul Ramesh{3}, Soo-Hyun Kim{3}
{1}Daegu Gyeongbuk Institute of Science and Technology, South Korea; {2}Tanaka Precious Metals, South Korea; {3}Yeungnam University, South Korea
4:50 pm - 4:55 pm
**PS-2-06. An All-Wet, Low Cost RDL Fabrication Process with Electroless Plated Seed/Barrier Layers**  
Ziru Cai, Yingtao Ding, Zhaohu Wu, Ziyue Zhang, Yuwen Su, Zhiming Chen  
Beijing Institute of Technology, China

4:55 pm - 5:00 pm
**PS-2-07. Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition on Silicon**  
Cheng-Hsuan Kuo\{3\}, Victor Wang\{3\}, Zichen Zhang\{3\}, Seonguk Yun\{3\}, Jeffrey Spiegelman\{1\},  
Daniel Alvarez\{1\}, Harsono Simka\{2\}, Andrew Kummel\{3\}  
\{1\}Rasirc, United States; \{2\}Samsung, United States; \{3\}UCSD, United States

5:00 pm - 5:05 pm
**PS-2-08. Impact of Nanosecond Laser Anneal on PVD Ru Films**  
Devika Sil\{1\}, Yasir Sulehria\{1\}, Oleg Gluschenkov\{1\}, Takeshi Nogami\{1\}, Roger Cornell\{1\},  
Andrew Simon\{1\}, Juntao Li\{1\}, Bala Haran\{1\}, Christian Lavoie\{1\}, Jean L Sweet\{1\}, Junjun Liu\{4\}, Karim Huet\{2\}, Fulvio Mazzamuto\{3\}  
\{1\}IBM Research, United States; \{2\}Laser Systems & Solutions of Europe, France; \{3\}Laser Systems & Solutions of Europe, Gennevilliers, France; \{4\}Screen, Albany, United States

5:05 pm - 5:10 pm
**PS-2-09. Development of Manganese Nitride Resistor with Near-Zero Temperature-Coefficient of Resistance to Achieve High-Thermal-Stability ICs**  
Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka  
Tohoku University, Japan

5:10 pm - 5:15 pm
**PS-2-10. Design of an Integrated III-V on Silicon Semiconductor Laser for Spiking Neural Networks**  
Keshia Mekemeza Ona, Benoit Charbonnier, Karim Hassan  
CEA-Leti, Université Grenoble Alpes, France

5:15 pm - 5:20 pm
**PS-2-11. Virtual Metrology Equipped with a Variability Analyzer in Chemical Mechanical Polishing**  
Lingyen Yeh, Shu Chun Huang  
Sun Innovation Co., Ltd., Taiwan
5:20 pm - 5:25 pm
PS-2-12. Interconnects Variability Control for High Voltage Applications
Kwang Sing Yew, Yi Jiang, Wanbing Yi, Ramasamy Chockalingam, Ran Xing Ong, Bo Li, Juan Boon Tan
GlobalFoundries, Singapore

5:25 pm - 5:30 pm
PS-2-13. A Study on the nitridation of Barrier Liner Contribution to Galvanic Corrosion of Copper bondpad
Xiaodong Li, Ramasamy Chockalingam, Poh Chuan Ang, Wah Peng Neo, Juan Boon Tan
globalfoundries singapore, Singapore

5:30 pm - 5:45 pm
Poster Session 2 - Authors Interview
Friday, July 9, 2021
8:00 am – 10:15 am  Session 7: Advanced Interconnect
Session Chairs:

8:00 am - 8:30 am
S7-1. Invited Speech: EM performance improvements for Cu interconnects with Ru-based liner and Co cap in advanced nodes
Koichi Motoyama
BEOL Metal Integration, IBM Research

8:30 am - 8:55 am
S7-2. XPS Diffusion Analysis of Ta(N)/Ru Diffusion Barriers for Cobalt Interconnects
Bettina Wehring, Lukas Gerlich, Benjamin Uhlig
Fraunhofer IPMS, Germany

8:55 am - 9:20 am
S7-3. Exploring W-Cu Hybrid Dual Damascene metallization for Future Nodes
Marleen van der Veen{2}, Olalla Varela Pedreira{2}, Nancy Heylen{2}, Nicolas Jourdan{2}, Stéphane Larivière{2}, Seongho Park{2}, Herbert Struyf{2}, Zsolt Tőkei{2}, Wei Lei{1}, Shirish Pethe{1}, Shinjae Hwang Feng Chen{1}, Zhiyan Wu Jérôme Machillot{1}, An
{1}Applied Materials Inc., United States; {2}imec, Belgium

9:20 am - 9:45 am
S7-4. Selective Deposition of AlOx for Fully Aligned via in Nano Cu Interconnects
Son Nguyen{2}, Hosadurga Shobha{2}, Corneliu Peethala{2}, Thomas Haigh{2}, Huai Huang{1}, Juntao Li{2}, James Demarest{2}, Balasubramanian Pranatharthi Haran{2}, Dennis Hausmann{3}, Paul Lemaire{4}, Kashish Sharma{3}, Pankaj Ramanì{3}, Arpan Mahorowala{3}
{1}IBM Research Center, United States; {2}IBM Research center, United States; {3}Lam Research, United States; {4}Lam Ressearch, United States

9:45 am - 10:10 am
S7-5. Aluminide Intermetallics for Advanced Interconnect metallization: Thin Film Studies
Jean-Philippe Soulie, Zsolt Tőkei, Johan Swerts, Christoph Adelmann
Imec, Belgium

10:10 am - 10:15 am
Next Conference Announcement

10:15 am – 10:30 am
Break
**Friday, July 9, 2021**

**10:30 am – 12:50 pm  Session 8: RC Scaling/Reliability**

Session Chairs:

10:30 am - 11:00 am  
**S8-1. Invited Speech:**  
Mauro Kobrinsky  
Intel

11:00 am - 11:30 am  
**S8-2. Invited Speech: Reliability Characterization on Advanced FinFET Technology**  
Kihyun Choi  
Samsung Electronics, South Korea

11:30 am - 11:55 am  
**S8-3. Reliability of Barrierless PVD Mo**  
Davide Tierno, Maryam Hosseini, Marleen van der Veen, Anish Dagol, Kristof Croes, Steven Demuynck, Zsolt Tőkei, Eugenio Dentoni Litta, Naoto Horiguchi  
imec, Belgium

11:55 am - 12:20 pm  
**S8-4. Joule Heating Investigation for Advanced Interconnect Schemes with airgaps**  
Melina Lofrano, Olalla Varela Pedreira, Ivan Ciofi, Herman Oprins, Seongho Park Park, Zsolt Tokei  
imec, Belgium

12:20 pm - 12:45 pm  
**S8-5. Effects of Composition Deviation of CuAl2 on BTS and TDDB Reliability**  
Toshihiro Kuge, Masataka Yahagi, Junichi Koike  
Tohoku University, Japan

12:45 pm - 12:50 pm  
Next Conference Announcement

12:50 pm - 1:00 pm  
Break

1:00 pm - 2:00 pm  
**Exhibitor Presentation 3**
Friday, July 9, 2021
2:00 pm – 4:20 pm  Session 9: DTCO/Novel System & Closing Remarks

Session Chairs:

2:00 pm - 2:30 pm  
**S9-1. Invited Speech: Technological Influences in Designing and Building a Wafer Scale Interconnect**  
Gary Lauterback  
CTO and Co-Founder, Cerebras Systems

2:30 pm - 3:00 pm  
**S9-2. Invited Speech: Resistive memories for neuromorphic hardware**  
Ms. Elisa Vianello  
senior scientist, CEA-Leti, France

3:00 pm - 3:25 pm  
**S9-3. Advanced CMP Process Control by Using Machine Learning Image Analysis**  
Min-Hsuan Hsu, Chih-Chen Lin, Hsiang-Meng Yu, Kuang-Wei Chen, Tuung Luoh, Ling-Wuu Yang, Ta-Hone Yang, Kuang-Chao Chen  
Macronix International Co. Ltd., Technology Development Center, Taiwan

3:25 pm - 3:50 pm  
**S9-4. Two-Level MOL and VHV Routing Style to Enable Extreme Height Scaling Beyond 2nm Technology Node**  
Bilal Chehab, Odysseas Zografos, Eugenio Dentoni Litta, Zubair Ahmed, Pieter Schuddinck, Doyoung Jang, Geert Hellings, Alessio Spessot, Pieter Weckx, Julien Ryckaert  
IMEC, Belgium

3:50 pm - 4:15 pm  
**S9-5. Novel IR/EM-Aware Power Grid Design and Analysis Methodologies for Optimal PPA at Sub-10nm Technology Nodes**  
Grant Miller, Saurabh Jain, Santosh Kelgeri, Pranav Raganathan, Ahmet Ceyhan  
Advanced Design, United States

4:15 pm - 4:20 pm  
Closing Remarks